REMARKS

The first amendment in the paragraph at page 9, lines 13-21 corrects a clerical error; the circuit 100 shown in Figure 2A has 324 column electrodes, as correctly shown in Figure 2A (Y001-Y324 cf. page 11, lines 22-23) and as stated at page 10, line 4. The second amendment in this paragraph simply moves the final period outside the parentheses.

The amendment in the paragraph bridging page 9 and 10 removes a parenthetical statement which is both wrong and inconsistent with page 13, lines 15-17; as correctly stated on page 13, the difference between the 32 possible outputs of each multiplexing unit 111 and the 31 possible output voltages provided on the voltage rails is accommodated by permitting two different outputs of a multiplexing unit to both select the Vcom voltage rail, and Vcom is not necessarily zero.

The amendments on page 13 simply correct two clerical errors; the original reference to Figure 1B is obviously erroneous since the multiplexing units 111 are not shown in Figure 1B but only in Figure 2B.

The amendment on page 15 corrects an inconsistency between that page and Figure 3A; as shown in Figure 3A, it is the voltage rail 215b, not the voltage rail 215a, which carries the voltage Vcom.

The remaining amendments in the specification are corrections of minor clerical errors, the need for which is, in each case, obvious from the context.

Upon review of the Office Action, the undersigned attorney realized that the original claims of this application largely failed to define correctly applicant's contribution to the art and contained a considerable number of obscurities. These deficiencies require major rewriting of a large number of claims, especially since, in order to define correctly applicant's contribution to the art, it is necessary to direct the claims to combinations of integers different from those appearing in the original claims. Accordingly, the undersigned attorney considers it most convenient for both the

Examiner and himself to delete all the original claims and to provide a "clean" set of claims on which the further prosecution of this application can be based.

Claim 38 is generic to the embodiments of the invention shown in Figures 1A, 1B, 2A, 2B and 3A-3E, and basis for this claim is found, *inter alia*, in these Figures and the related portions of the Detailed Description. Specifically, it is believed that basis for this claim will readily be apparent from the following annotated version thereof:

An addressing structure [10, 100, 200] for addressing a display medium, the structure comprising:

a plurality of column electrodes [Figure 1A, integer 18; Figure 2A, integers Y001-Y324, and page 11, lines 22-23; Figure 3A, integer 18a], each of the column electrodes [18] being connected via switch means [22] to a plurality of pixel electrodes [23];

a plurality of voltage sources [Figure 1A, integer 14, Figure 2A, integer 150] each having a different voltage level; and

a switch unit [Figure 1A, integer 12, Figure 2A, integer 110] having a plurality of voltage source inputs each connected to one of the plurality of voltage sources [14, 150] , and a plurality of outputs each connected to one of the plurality of column electrodes [18, Y001-Y324], the switch unit being capable of connecting each of the column electrodes independently to selected ones of the plurality of voltage sources [Figure 2B, units 111, and associated description on pages 12-13, especially page 13, lines 13-15].

Claim 39 is directed to an addressing structure according to claim 38 wherein the switch unit further comprises at least one display signal input [Figure 1A, integer 13, Figures 2A and 2B, lines connecting data latch 120 to switch unit ("power rail selector") 110] arranged to receive a display signal specifying the voltages to be placed upon column electrodes, and the switch unit is arranged to connect each of the column electrodes independently to selected ones of the plurality of voltage sources dependent upon the display signal [see page 10, lines 16-22 and page 13, lines 7-17].

Claim 40 is directed to an addressing structure according to claim 39 wherein the switch unit comprises one display signal input for each column electrode and the switch unit is arranged to connect each column electrode to a selected one of the plurality of voltage sources dependent upon the display signal received by the display signal input associated with the column electrode. Basis for this claim is found, *inter alia*, in Figure 2B and the related description; note that each multiplexing unit 111 receives a single output from the data latch 120 and controls a single one of the column electrodes Y001-Y324.

Claim 41 is directed to an addressing structure according to claim 39 further comprising a data register for receiving sequentially data representing voltages to be applied to each of the column electrodes, and for storing said data, and data latching means for receiving said data from the data register, the at least one display signal input being connected to the data latching means. Basis for this claim is found, *inter alia*, in Figure 2A and the related description relating to the data register 130 and the data latch 120; note that, in so far as the switch unit 110 is concerned "the at least one display signal input" comprises the outputs from the data latch 120.

Claim 42 is directed to an addressing structure according to claim 38 wherein the switch unit comprises a plurality of multiplexing units, one multiplexing unit being connected to each column electrode, each multiplexing unit comprising a number of switches equal to the number of voltage sources inputs of the switch unit, each switch being capable of connecting its associated column electrode to its associated voltage source input, the multiplexing units being arranged to that, in each multiplexing unit only one of the switches is closed at any given time, all the other switches being open. Basis for this claim is found, *inter alia*, in Figure 2B and the related description, especially page 13, lines 7-17.

Claim 43 is directed to an addressing structure according to claim 38 wherein the switch unit further comprises a blanking signal input arranged to receive a blanking signal, the switch unit being arranged to that, upon receipt of the blanking

signal, all column electrodes are connected to the same voltage source. Basis for this claim is found, *inter alia*, in Figure 2A and the related description, especially page 11, lines 24-25, which describes how the blanking signal input BL in Figure 2A is used to set all the column electrodes Y001-Y324 to the same voltage source, namely that providing voltage Vcom.

Claim 44 is directed to the embodiment of the invention shown in Figures 3A-3E which is, as stated at page 14, lines 2-4, a special form of the broad invention shown in Figure 1A. Basis for this claim is found, *inter alia*, in Figures 3A-3E and the related portions of the Detailed Description. Specifically, it is believed that basis for this claim will readily be apparent from the following annotated version thereof:

An addressing structure [Figure 3A, integer 200] according to claim 38 wherein the switch unit comprises a primary switch unit [212], a plurality of voltage rails [215a, 215b, 215c], a plurality of secondary switch units [210] each having an output connected to one column electrode [18a], and sequencing means [220], the primary switch unit [212] having voltage source inputs [inputs connected to lines 214] connected to the voltage source inputs of the switch unit, voltage rail outputs each connected to one voltage rail [215a, 215b, 215c], and at least one control signal input [see the broken lines connecting switch unit 212 to sequencing means 220] arranged to receive a primary switch unit control signal from the sequencing means [220], each secondary switch unit [210] having voltage rail inputs connected to each of the voltage rails [215a, 215b, 215c] and a control signal input [see the line connecting unit 210 to sequencing means 220] arranged to receive a secondary switch unit control signal from the sequencing means [220], the sequencing means [220] controlling the primary switch unit so that the voltage rails are connected to a first subset of the voltage source inputs of the primary switch unit during a first period, and to a second subset, different from said first subset, of the voltage source inputs of the primary switch unit during a second period [see especially page 15, lines 10-18, which describe how the positive and negative voltage rails 215a and 215c respectively are cycled from V to V/2 to V/4 to V/8 during successive sub-frames],

and each of the secondary switch units [210] being arranged to connect their associated column electrode [18a] to a selected one of the voltage rails [215a, 215b, 215c] dependent upon the secondary switch unit control signal [see especially page 15, lines 19-28; see also the detailed description of Figures 3C to 3E at page 17, lines 10-22].

Claim 45 is directed to an addressing structure according to claim 44 wherein one voltage rail [215b] is maintained at the same voltage [Vcom] during the first and second periods [see page 15, lines 15-16, which describe how voltage rail 215b is maintained at Vcom throughout the operation of the addressing structure 200].

Although the terms "primary switch unit" and "secondary switch unit" are not found *ipsissima verba* in the specification, the integer 212 in Figure 3A is identified as a switch unit, while the integer 210, identified as a "source driver" is stated to function as 'a "one-bit voltage rail switch circuit" (page 16, lines 3-4). Accordingly, the specification provides proper basis for referring to both integers as switch units discrete from one another, and the adjectives "primary" and "secondary" are used solely to distinguish the two integers to improve the ease of understanding of the claim.

Claim 46 is directed to an addressing structure according to claim 45 having at least three voltage rails [215a, 215b, 215c], a first voltage rail [215b] maintained at the same voltage [Vcom] during the first and second periods, a second voltage rail [215a, and see page 15, lines 16-18] maintained positive with respect to the first voltage rail [215b] during the first and second periods, and a third voltage rail [215c] maintained negative with respect to the first voltage rail [215b] during the first and second periods.

Claim 47 is directed to an addressing structure according to claim 44 wherein the sequencing means is arranged to receive a digital display signal comprising a plurality of digits defining the voltages to be applied to a given column electrode, and the sequencing means controls the secondary switch units such that the signal applied to that column electrode during the first period is defined by one digit of the digital display signal and the signal applied to that column electrode during the second period is defined

by a second digit of the digital display signal. Basis for this claim is found, *inter alia*, at page 16, lines 8-13 and Figures 3C to 3E, which describe how the individual digits of a binary number provided by the display signal fed to the sequencing means are used to control the voltage rail to which secondary switch unit 210 connects the column electrode 18a during each sub-frame.

Claim 48 is directed to an addressing structure according to claim 44 wherein the voltage sources comprise a voltage source Figure 3A, integer 240] having a central voltage [Vcom] at which the voltage rail is maintained during the first and second periods, a predetermined number of voltages [+V, +V/2, +V/4, +V/8] greater than the central voltage [Vcom] and the same predetermined number of voltages [-V, -V/2, -V/4, -V/8] less than the central voltage [Vcom].

Claim 49 is directed to an addressing structure according to claim 48 wherein the differences between the central voltage and the predetermined number of voltages greater than the central voltage form a geometric series 1, 2, 4 etc. and the differences between the central voltage and the predetermined number of voltages less than the central voltage form a similar geometric series. It is believed that the basis for this claim will readily be apparent from the preceding paragraph.

Claim 50 is directed to an electro-optic display incorporating an addressing structure according to claim 38. It is believed that basis for this claim will readily be apparent from the following annotated version thereof:

An electro-optic display comprising:

a transparent substrate bearing a single transparent common electrode [page 13, lines 23-24];

an addressing structure according to claim 38; and

an electro-optic medium disposed between the pixel electrodes of the addressing structure and the common electrode, the common electrode extending across all the pixels of the display [page 13, lines 24-26].

Claim 51 is directed to an electro-optic display according to claim 50 wherein the switch unit of the addressing structure comprises a blanking signal input arranged to receive a blanking signal, the switch unit being arranged so that, upon receipt of the blanking signal, all column electrodes are placed at the same voltage as the common electrode. It is believed that the basis for this claim will readily be apparent from the explanations of the bases for claims 39 and 50 above. Similarly, it is believed that the basis for claim 52 will readily be apparent from the explanations for the bases of claims 44 and 50 above.

Claim 53 is essentially directed to a method of operating the display of claim 38 and it is believed that the basis for this claim will readily be apparent from the explanation of the basis for claim 38 above. Similarly, claims 54, 55 and 56 are directed to methods according to claim 53 having additional features corresponding to those of claims 41, 39 and 44 respectively, and the bases for claims 54, 55 and 56 will readily be apparent from the explanations of the bases for claims 41, 39 and 44 respectively given above.

Claim 57 is directed to the method of addressing a display medium illustrated in Figures 4A, 4B and 5A-5E, and is essentially a revised version of the former claim 17. The major differences between the language used in claim 57 and that previously used in claim 17 are largely attributable to a determination by the undersigned attorney that the differences between the method of claim 57 and the prior art are such that the invention may most readily be claimed in terms of a method in which one column electrode is arranged to carry out the method of (say) Figure 5C, while a second column electrode is arranged to carry out a different method (say) that of Figure 5D.

The basis for the second paragraph of claim 57 will first be explained. The first column electrode, although not specifically identified as such, is the electrode on which the voltage Vd(t) is present; note that page 19, lines 20-21 state that this voltage "may be a column drive voltage directed to a column of pixels" which by definition makes the line carrying this voltage a column electrode. Similarly, although Figure 4A

does not explicitly illustrate a pixel electrode, page 19, line 25 states that the capacitive element 335 in turn applies a voltage Vp(t) to the pixel unit, i.e., to the pixel electrode. In the second paragraph of claim 57, the first capacitor is capacitive element 335 in Figure 4A, the first resistive switch means is the circuit 320 in the same Figure, and the portion of the claim relating to the open and closed positions of the switch are based upon page 19, lines 21-24. The third paragraph of claim 57 is exactly analogous to the second one and has the same basis.

The fourth paragraph of the claim is based upon page 19, lines 21-24; in any case, it is surely inherent that the switches must be closed to enable the drive voltage to be transmitted from the column electrodes to the capacitors. The fifth paragraph of the claim is based upon, for example, Figure 5C, in which application of the drive voltage Vd3 for the (first) period from t4 to t5 results in an addressing voltage Vp3 different from the drive voltage. The last paragraph of claim 56 is based upon, for example, Figure 5D, in which application of the drive voltage Vd4 (equal to Vd3) for a (second) period from t3 to t5 results in an addressing voltage Vp4 different from both Vd4 and Vp3.

Claim 58 is directed to a method according to claim 57 in which the first and second periods are multiples of a predetermined interval. This claim is based upon, *inter alia*, Figures 5B, 5C and 5D which illustrate application of the drive voltage for respectively 4, 1 and 2 of the equal-length sub-frames.

Claims 59 and 60 are apparatus claims directed to apparatus for carrying out the methods of claims 57 and 58 respectively, and it is believed that the basis for claims 59 and 60 will readily be apparent from the foregoing explanations of the bases for claims 57 and 58.

No new matter is introduced by any of the foregoing amendments.

Claims 33-37 were rejected under 35 USC 112, second paragraph as being indefinite on the grounds that it is not clear why the addressing voltage is less than a voltage level of the voltage source at the end of the period since the resistive switch is turned on for a period of time. While technically this rejection is moot in view of the

cancellation of claims 33-37, the following explanation is provided in view of the presence of somewhat similar language in new claims 57 and 59.

As mentioned (perhaps with less than optimal clarity) at page 20, lines 21-28 of the specification, in an active matrix display in which pixel electrodes are connected to capacitors and, via switches (typically FET's) to column electrodes, when the FET for a particular pixel is turned on, the resistance of the FET and the capacitor form an RC circuit which causes the voltage on the pixel electrode ("the pixel electrode voltage" or "PEV") to increase gradually for a period after a drive voltage is applied to the column electrode, generally in the manner illustrated in the lower part of Figure 5B of this application. In the prior art, the values of the resistance and capacitance are typically such that the rise in the pixel electrode voltage is rapid and for practical purposes the PEV is the same as the drive voltage. In such a prior art system, any modulation of the PEV needed, for example for gray level control in an LCD, must be provided by voltage modulation of the drive voltage.

However, in accordance with the present invention, it is possible to vary the resistance and capacitance of the RC circuit so that the rise in the PEV is more gradual. If the drive voltage applied to any column electrode is now pulse width modulated (i.e., the period for which a constant drive voltage is applied to the column electrode is varied) so that the drive voltage is terminated before the PEV approaches the drive voltage, it is possible to cause the PEV to adopt varying values less than the drive voltage, as illustrated for example in Figures 5C and 5D. Hence, in the method of new claim 57, the first and second addressing voltages (PEV's) are both different from the drive voltage and from each other.

The last sentence of Section 1 of the Office Action is moot, since there is no similar language in any of the present claims.

Although the 35 USC 102 and 103 rejections in Sections 2-4 of the Office Action are technically moot since all the original claims have been cancelled, the following explanation if offered as to why the new claims filed herewith are patentable

over the references of record. Various claims were rejected as anticipated by Proebsting, U.S. Patent No. 5,952,948. Proebsting describes a conventional active matrix liquid crystal display having an addressing structure or backplane (Proebsting, Figure 1) having a shift register and data latch which function in a manner generally similar to the corresponding integers in Figure 2A of the present application. The outputs from Proebsting's data latch are fed to separate digital/analogue converters, which in turn supply drive voltages to the column electrodes of the conventional active matrix display, these column electrodes being connected via transistors 110 to pixel electrodes 112. As the Office Action correctly notes, the internal circuitry of each of Proebsting's DAC's shown in his Figure 2 includes a multiple-tap transformer and a series of resistors which provide a series of voltage sources each having a different voltage level, and switch means (204) for connecting any desired one of these voltage sources to the column electrode.

The main difference between Proebsting and present claims 38-56 is that in Proebsting's backplane, each DAC generates its own series of voltage sources, so that any given series of voltage sources only supplies voltage to one column electrode. In contrast, in the addressing structure of present claims 38-56, a single switching unit 12 or 110 connects a single set of voltage sources 14 or 150 to a plurality of column electrodes 18 or Y001-Y324. Similarly, neither Kageyama et al. nor Reddy describe such a switching unit. For similar reasons, none of the references of record describe a method in accordance with any of present claims 53-56.

Furthermore, with reference to present claims 44-49 and 56, none of the references of record describe a switching unit having a primary switching unit, voltage rails and secondary switching units as defined in claims 44 and 56.

With reference to present claims 57-60, none of the references of record describe the use of pulse width modulation of a drive voltage applied to an RC circuit in order to produce a varying addressing voltage on a pixel electrode, as required by present

claims 57-60; in all the references of record it appears that the addressing voltage becomes, essentially instantaneously, equal to the drive voltage.

For the foregoing reasons, all of the claims remaining in this application are patentable over the references of record. Accordingly, reconsideration and allowance of all remaining claims is respectfully requested.

This application now contains 23 claims, including 4 independent claims, while applicants have previously paid fees for 37 claims, including 4 independent claims. Accordingly, no additional claim fees are required by the Amendment. However, since the normal period for responding to the Office Action expired December 21, 2005, a Petition for a two-month extension of this period is filed herewith.

Respectfully submitted

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